Amendments to the Specification:

Page 14, Line 8:

Fig. 5A depicts a second embodiment of a portion of an MRAM 200 in accordance with the present invention. Fig. 5B depicts a cross-sectional view of the second embodiment of a portion of the MRAM 200 in accordance with the present invention. Referring to Figs. 5A and 5B, the MRAM 200 includes selection devices 208 and 210, which are preferably CMOS transistors. The structure 210 is isolated from like structures using dielectric trenches 204 and 206 in the substrate 202. The structure 200 includes two memory cells using two MTJ stacks 11. The CMOS transistor 210 includes a source 213, drains 212, and a gate 215. The CMOS transistor 208 includes the source 213, drain 214, and gate 217. A metal plug 216 connects the source 213 to ground conductor 218. Metal plugs 219 and 220 connect the drains 212 and 214, respectively, to the bottom electrodes 223 and 224 for the MTJ stacks 11. The write bit lines 221 and 222 reside below the MTJ stacks11. The write word line ~~226~~ 225 is oriented at an angle to the bit lines 221 and 222. The MRAM 200 also includes insulating layer 226 and soft magnetic layer 228. The insulating layer 226 and soft magnetic layer 228 correspond to the layers 124 and 130, respectively, depicted in Fig. 4. Referring back to Figs. 5A and 5B the insulating layer 226 and soft magnetic layer 228 function in a similar manner to the insulating layer 124 and soft magnetic layer 130. In particular, the insulating layer 226 resides on the sides and tops of write word lines 225 and 234. The soft magnetic layer 228 is insulated from the write word lines 225 and 234 using the insulating layer 226. The soft magnetic layer 228 concentrates the magnetic flux below the lines 225, and 234. In other words, the portion of the soft magnetic layer 228 on the surfaces of lines 225, and 234 increases the magnetic field in the space underneath write bit

lines 225 and 234 and in proximity to the free layer 1103 by reducing the magnetic field around other portions of the lines 225 and 234. Consequently, the write efficiency of write line 225 is improved.